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An oxidation-last annealing for enhancing the reliability of indium-gallium-zinc oxide thin-film transistors

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The dependence of device reliability against a variety of stress conditions on the annealing atmosphere was studied using a single metal-oxide thin-film transistor with thermally induced source/drain regions. A cyclical switch between an oxidizing and a non-oxidizing atmosphere induced a regular change in the stress-induced shift of the turn-on voltage, with the magnitude of the shift being consistently smaller after annealing in an oxidizing atmosphere. The observed behavior is discussed in terms of the dependence of the population of oxygen vacancies on the annealing atmosphere, and it is recommended the last of the sequence of thermal processes applied to a metal-oxide thin-film transistor be executed in an oxidizing atmosphere. *Published by AIP Publishing.* [http://dx.doi.org/10.1063/1.4979649]

Metal-oxide (MO) thin-film transistors (TFTs), such as those based on indium-gallium-zinc oxide (IGZO), are deployed in advanced flat-panel displays.[1] While requiring manufacturing infrastructure largely compatible with their amorphous silicon based counterparts, they exhibit better device characteristics, such as higher field-effect mobility (μ_{FE}) and lower leakage current.[2]

Much has been reported on the effects of thermal processes on the characteristics of MO TFTs.[3–10] The influence of the annealing atmosphere (such as inert,[3–5] air,[6,7] oxidizing,[8,9] or water vapor[10]) on device reliability is often compared across different TFTs. The inherent statistical variation of the device attributes in these studies complicates the effort to draw definite conclusions on how different thermal processes affect the characteristics and reliability of a TFT. Consequently, there is a lack of a generally agreed approach to the thermal processing of a MO TFT.

In this work, MO TFTs with thermally induced source/drain (S/D) regions[11] were constructed. The effects of annealing in an inert or oxidizing atmosphere on device reliability were compared using a single TFT, thus eliminating the confounding effects of the statistical variation alluded to earlier. A variety of stress conditions have been studied, including negative/positive bias stress without (N/PBS) and with illumination (N/PBIS).

Since the annealing was performed at the end of the process flow and after the metallization, any observable effects could be unambiguously attributed to the annealing process: including the regular change in the stress-induced shift (ΔV_{on}) in the turn-on voltage (V_{on}) of the TFT resulting from a cyclical switch between an oxidizing and an inert annealing atmosphere. It was observed that a correlation existed between a negative shift in the initial V_{on} and a larger magnitude of ΔV_{on}—hence degraded reliability. A possible mechanism is discussed, based on the dependence of the population of oxygen vacancies (V_O) on the annealing atmosphere. In the absence of other potential issues of process incompatibility, it is recommended that the last of the sequence of thermal processes applied to an MO TFT be executed in an oxidizing atmosphere.

The fabrication of the TFTs started with the sputtering and patterning of ~50 nm indium-tin oxide as the bottom gate electrode on an oxidized silicon wafer. Following a 420 °C plasma-enhanced chemical vapor deposition (PECVD) of 100 nm silicon oxide (SiO_x) as the gate dielectric, a ~25 nm IGZO active layer was deposited by radio-frequency magnetron sputtering at ambient temperature using an IGZO target with a molar ratio of In_2O_3:Ga_2O_3:ZnO = 1:1:1. The sputtering atmosphere was 10% oxygen (O_2) and 90% argon, at a process pressure of 3 mTorr. The patterned active islands were subsequently capped with a double-layer consisting of 100 nm gas-impermeable silicon nitride (SiN_y) on 300 nm permeable SiO_x, respectively, deposited via PECVD at 300 °C and 420 °C. With the SiO_x serving as an etch-stop and a passivation layer, the SiN_y covering the channel region was removed in a reactive-ion etcher. After the contact holes were opened, a sputtered aluminum/molybdenum (Al/Mo) bilayer was patterned to form the electrodes. Highly conductive S/D regions were subsequently thermally "activated" at 400 °C in O_2 for 3.5 h.[11] Shown in Figs. 1(a) and 1(b) are the respective schematic diagram and cross-sectional scanning-electron micrograph of the resulting TFT with thermally induced S/D regions.

The performance and reliability of the TFTs were characterized using an Agilent 4156C Semiconductor Parameter Analyzer. Additional annealing schedules were performed on the same set of TFTs at 350 °C in nitrogen (N_2) and subsequently at 400 °C in O_2. All annealing schedules were carried out at atmospheric pressure. The reliability was assessed after each annealing schedule.

Shown in Fig. 1(c) are the transfer curves measured immediately after 3.5 h of S/D activation anneal. Defining the gate voltage (V_g) at which an exponential increase in the drain current (I_d) is first observed, a V_{on} of ~−1.5 V was obtained. Also extracted were a peak μ_{FE} of ~5 cm^2/V s, a

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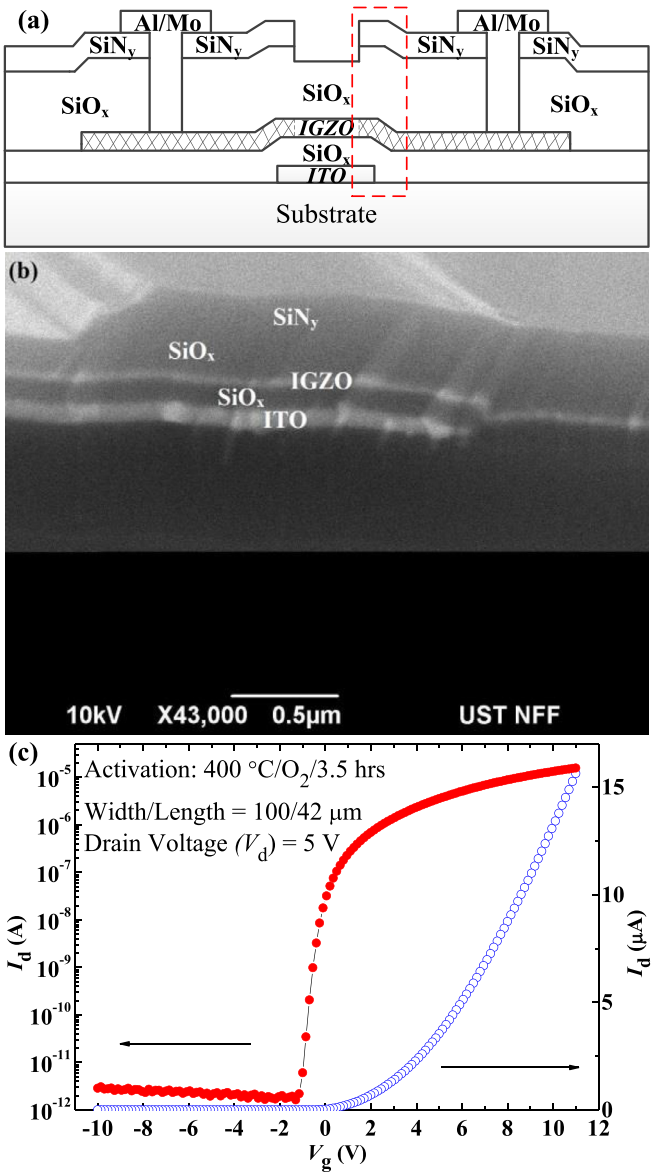

FIG. 1. (a) The schematic cross-section of the IGZO TFTs with thermally induced and highly conductive S/D regions (cross hatched). (b) High-resolution cross-sectional scanning-electron micrograph taken around the location outlined by the red box in (a). (c) The transfer curves of the as-fabricated IGZO TFT in both the logarithmic (solid: left axis) and linear (hollow: right axis) scales.

pseudo-subthreshold swing of ~200 mV/decade, and an on-off current ratio of over 10^7.

Four TFTs were subjected to NBS, NBIS, PBS, and PBIS tests for 10 000 s, during which V_g shifted from the initial V_{on} by −20 and +20 V was applied for the respective negative and positive bias stress; the S/D electrodes were grounded. The illumination tests were conducted using filtered 2.48 eV light (wavelength ~ 500 nm) at a power density of 0.2 W/m^2 measured using a calibrated photo-diode. Referenced to the V_{on} measured prior to the stress tests, the dependence of ΔV_{on} on the stress time is plotted in Fig. 2.

For NBS, PBS, and PBIS, ΔV_{on} only fluctuates within a narrow band between ±0.15 V. This implies that V_{on} was minimally affected by the stress since 0.15 V was the voltage step used during the measurement of the transfer curves.

Consistent with previous reports, a continuous negative shift in V_{on} was observed during NBIS and up to ~ −1.8 V

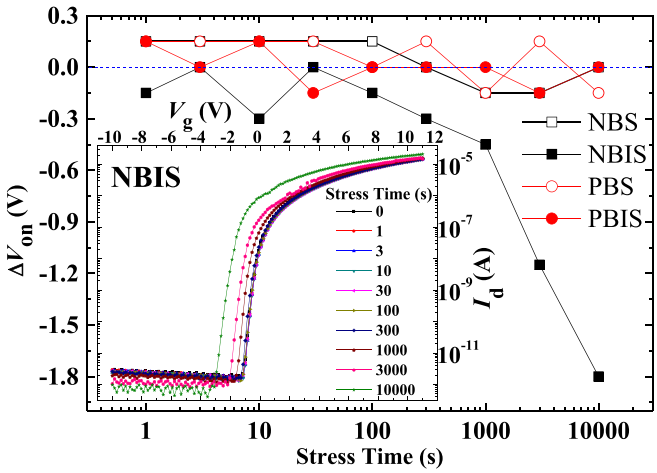

FIG. 2. The dependence of ΔV_{on} on the stress time for IGZO TFTs subjected to N/PBS and N/PBIS. Shown in the inset is the time-evolution of the transfer characteristics under NBIS.

after 10 000 s. It has been reported that long-living excess electrons[12] can be generated by the photo-ionization of oxygen vacancies (V_O): $V_O + h\nu \rightarrow V_O^{2+} + 2e^-$ when IGZO is illuminated by photons with the energy ($h\nu$) above 2.3 eV,[13,14] thus resulting in persistent photo-conductivity and possibly accounting for the observed negative shift in V_{on}. However, the absence of an obvious ΔV_{on} during identically illuminated PBIS strongly indicates that photo-electron generation alone was not responsible for the observed NBIS-induced ΔV_{on}. An additional mechanism is the drift of photo-generated holes and their subsequent accumulation in the traps at the gate dielectric/channel interface.[15–18] Due to its screening by the field-induced electron accumulation layer, the electric field responsible for such hole drift in the bulk of the channel region is significantly attenuated during PBIS.

Defects generated in the stressed TFTs were first removed by an oxidizing anneal at 400 °C for 30 min in O_2 before the TFTs were subsequently annealed at 350 °C for 5 min in N_2. The stress tests were repeated, and the effects on ΔV_{on} resulting from this non-oxidizing anneal are shown in Fig. 3(a).

Stress-induced negative ΔV_{on} is consistently observed under all four stress conditions in Fig. 3(a), with the corresponding magnitudes larger when the stress bias was negative. This is consistent with an increase in the population of V_O after a non-oxidizing anneal.[9] This could lead to increased tunneling of electrons from the valance band to the conduction band, which is mediated by the larger population of V_O. It was the subsequent drift and capture of these holes that was responsible for the higher NBS-induced ΔV_{on}. The population of holes is further increased under illumination, resulting from the V_O-modulated photo-generation of holes. This accounts for the even larger ΔV_{on} for NBIS than NBS. Again, the stress-induced ΔV_{on} was attenuated when the bias was positive, due to the screening effect of the field-induced channel charge.

The same TFTs were subsequently subjected to an oxidizing anneal at 400 °C for 0.5 h in O_2 after N_2 annealing. The resulting ΔV_{on} is compared in Fig. 3(a) with that measured after the two previous stress tests. The significant

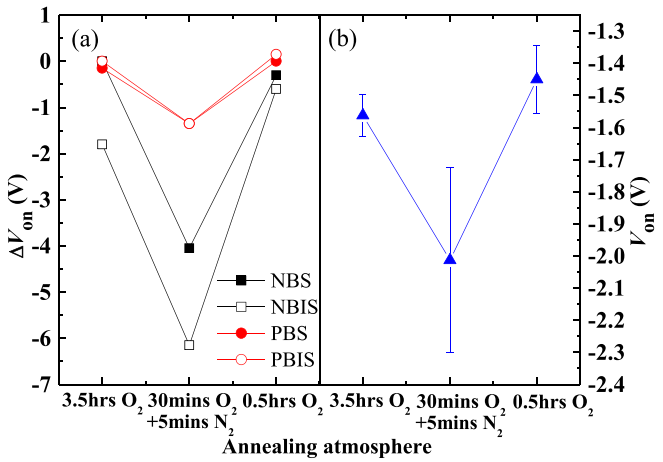

FIG. 3. The dependence on a cyclical change ($O_2/N_2/O_2$) in the annealing atmosphere of (a) ΔV_{on} measured at the end of 10 000 s stress tests and (b) the pre-stress V_{on}.

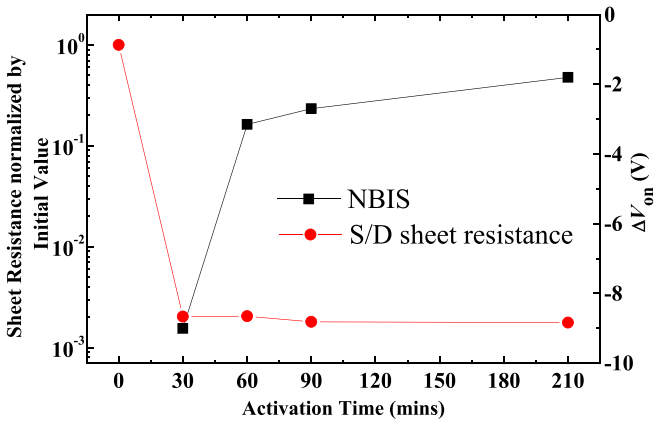

FIG. 4. The dependence on the activation annealing time of the NBIS-induced ΔV_{on} and the sheet resistance of the thermally induced S/D regions of IGZO TFTs.

reduction in the magnitude of the stress-induced ΔV_{on} is a strong indication of the effectiveness of the oxidizing anneal in reducing the population of V_O and with it also the population of holes.

Since V_O are known donor-defects, their presence in the channel has also been reported to result in a negative shift in V_{on}. Plotted in Fig. 3(b) is a comparison of the initial V_{on} measured immediately after each thermal cycle and before the stress tests. The more negative V_{on} measured after the non-oxidizing anneal is consistent with an increased population of V_O. Therefore, it is not surprising that a correlation exists between a negative shift in the pre-stress V_{on} and a larger magnitude of stress-induced ΔV_{on}. The significant recovery of V_{on} (Fig. 3(b)) upon oxidizing annealing indicates the absence of cumulative effects from the previous stress tests.

For a TFT with thermally induced S/D regions, the "activation" of the S/D regions and the oxidizing annealing of the channel region are accomplished simultaneously during the post-metallization oxidizing thermal treatment.[11] The duration of the treatment is constrained by the desire to achieve an adequately low resistance in the S/D regions and a sufficient reduction in the population of V_O in the channel. The dependence of both the stress-induced ΔV_{on} after 10 000 s NBIS (the most severe of the 4 stress conditions) and the normalized S/D sheet resistance on the activation annealing time at 400 °C in O_2 was investigated and is plotted in Fig. 4.

It can be seen that both the normalized S/D resistance measured using a standard cross-bridge structure and the magnitude of the stress-induced ΔV_{on} decrease with increasing annealing time, with the time to reach the respective saturation values being shorter for the former (~30 min) than for the latter (~60 min). Because of the desire to reduce both device attributes, the duration of the annealing time is constrained by the process with the slower dynamics, i.e., the reduction in the magnitude of ΔV_{on}. Consequently, an initial annealing time of 210 min (3.5 h) was selected.

The dependence of the population of V_O on the annealing condition was verified using x-ray photoelectron spectroscopy (XPS). Bare IGZO samples without oxide covers were subjected to the same annealing sequences as the TFTs. It has been revealed in previous work that an oxide cover merely changes (in fact slows down[11]) the oxidation of the IGZO. Therefore, the overall effect, in terms of the generation and annihilation of oxygen vacancies, remains the same. Shown in Fig. 5 are the measured O 1s spectra of the as-deposited IGZO (Sample A) and samples annealed for 1 h in O_2 at 400 °C (Sample B), for 4 h in O_2 at 400 °C (Sample C), and for an additional 5 min in N_2 at 350 °C after 4 h in O_2 at 400 °C (Sample D).

After the removal of surface contaminates (such as dissociated O_2 or other adsorbed species like -OH, $-CO_3$, H_2O, or O_2)[19,20] using *in situ* argon ion bombardment, each calibrated spectrum can be nicely resolved into two Gaussian–Lorenz

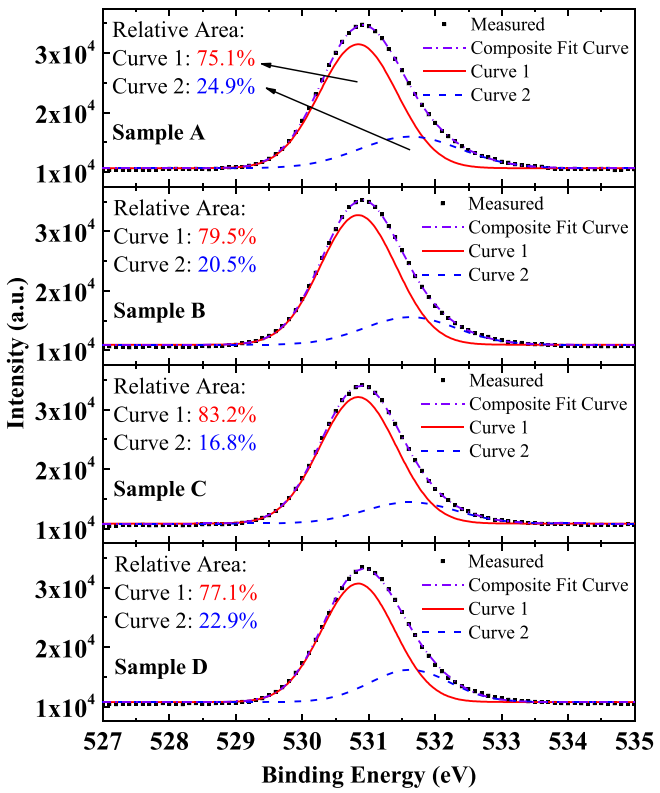

FIG. 5. The XPS spectra of O 1s in the IGZO films subjected to different annealing conditions, together with the Gaussian–Lorentz decompositions.

components—and labelled as "Curve 1" and "Curve 2" centered, respectively, at ~530.8 and ~531.6 eV. The former is associated with the O^{2-} ions at their native sites in fully oxidized stoichiometric IGZO,[20–22] and the latter is attributed to O^{2-} ions or OH species located in an oxygen-deficient In-Ga-Zn-O bonding matrix. Normalized by the total area of the corresponding composite spectrum, the percentage area of the Curve 2 component is taken to be a measure of the population of V_O.[19,23]

Compared with that of Sample A, the percentage areas of Curve 2 (hence also the populations of V_O) in Samples B and C decreased with increasing oxidizing annealing time. The trend is reversed for Sample D, which was subjected to an additional non-oxidizing N_2 anneal. The change in the population of V_O from XPS is consistent with the dependence of ΔV_{on} and V_{on} on the annealing condition shown in Fig. 3.

The dependence of the reliability of IGZO TFTs with thermally induced S/D regions on post-metallization oxidizing and non-oxidizing annealing atmospheres has been studied using the same TFT, thus eliminating any confounding effects due to the statistical variation of the initial device attributes. A correlation has been found to exist between a negative shift in the pre-stress V_{on} and a larger magnitude of the stress-induced ΔV_{on}—hence degraded reliability. These shifts also correlate well with the dependence of the population of V_O on the annealing conditions. In the absence of other potential issues of process incompatibility, it is recommended the last of the sequence of thermal processes applied to an MO TFT be executed in an oxidizing atmosphere.

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